CLAIMS

What is claimed is:

1. A system for generating and acquiring pseudo-noise (PN) spread signals, the system comprising:

a transmitter, wherein the transmitter comprises:

a first clock generator,

at least three first pseudo-noise (PN) component code generators coupled to the first clock generator;

a logic combiner coupled to the at least three first PN component code generators, the logic combiner adapted to generate a composite PN code;

a first N-bit counter coupled to the first clock generator;

a second clock generator, wherein the second clock is adapted to synchronize with the first clock generator;

a second M-bit counter coupled to the second clock generator;

a receiver, the receiver adapted to receive signals from the transmitter, comprising:

a link control processor;

a modulator/demodulator controller coupled to the link control processor;

a first receiver clock generator;

at least three first receiver pseudo-noise (PN) component code generators coupled to the first receiver clock generator;

a despreader coupled to one of the at least three first receiver PN component code generators;

a receiver logic combiner coupled to the at least three first receiver PN component code generators, the receiver logic combiner adapted to generate the composite PN code;

a first receiver N-bit counter coupled to the first receiver clock generator;

a second receiver clock generator, wherein the second receiver clock generator is adapted to synchronize with the first receiver clock; and

a second receiver M-bit counter coupled to the second receiver clock generator.

2. A system as in claim 1 wherein the first clock generator comprises a first direct digital synthesizer.

3. A system as in claim 1 wherein the logic combiner comprises a MAND logic combiner.

4. A system as in claim 1 wherein the logic combiner comprises a MAJ logic combiner.

5. A system as in claim 1 wherein the at least three first PN component code generators comprise four first PN component code generators.

6. A system as in claim 1 wherein the at least three first receiver PN component code generators comprise four first receiver PN component code generators.

7. A system as in claim 1 wherein the second clock generator comprises a crystal reference oscillator.

8. A system as in claim 1 wherein the second clock generator comprises a stable clock reference having a stability greater than or equal to 1×10^{-7} parts per part per year.

9. A system as in claim 1 wherein the second receiver clock generator comprises a second crystal reference oscillator.

10. A system as in claim 1 wherein the second receiver clock generator comprises a stable clock reference having a stability greater than or equal to 1×10^{-7} parts per part per year.

11. A system as in claim 1 wherein the second N-bit counter coupled to the second clock comprises at least a 40-bit counter.

12. A system as in claim 1 wherein the second receiver N-bit counter comprises at least a 40-bit counter.

13. A method for generating and acquiring pseudo-noise (PN) composite spread signals, the method comprising the steps of:

at a transmitter:

providing a PN clock source, the PN clock source having a predetermined cycle rate;

using the PN clock source to generate at least three PN component codes, wherein the step of generating the at least three PN component codes further comprises the steps of:

initializing a first counter, wherein the first counter is adapted to count the PN clock source cycles;

logically combining the at least three PN component codes to produce a PN composite code;

providing an oscillatory reference source, the oscillatory reference source having predetermined cycles;

initializing a second counter, wherein the second counter is adapted to count the cycles of the oscillatory reference source;

determining a transmitter delta phase in accordance with counts from the first counter and the second counter;

PN composite coding the transmitter delta phase and the second counter count;

transmitting the PN composite coded transmitter delta phase and the PN composite second counter count at a predetermined rate;

at a receiver:

receiving the transmitted signal;

partially correlating the transmitted signal; and

determining a PN composite code slip for chip aligning a receiver PN composite code with the transmitter PN composite code.

14. A method as in claim 13 wherein the step of providing the PN clock source further comprises the step of providing a direct digital synthesizer.

15. A method as in claim 13 wherein the step of generating the at least three PN component codes further comprises the step of generating one of the at least three PN component codes with predetermined auto-correlation properties.

16. A method as in claim 13 wherein the step of generating at least three PN component codes further comprises the step of generating four PN component codes.

17. A method as in claim 16 wherein the step of combining the four PN component codes further comprises the step of MAND combining the four PN component codes according to:

$$(X \oplus (Y \bullet (Z_1 \oplus Z_2))$$

18. A method as in claim 16 wherein the step of combining the four PN component codes further comprises the step of MAJ combining the four PN component codes according to:

$$(X \bullet Y) \oplus (X \bullet Z_1) \oplus (X \bullet Z_2) \oplus (Y \bullet Z_1) \oplus (Y \bullet Z_2) \oplus (Z_1 \bullet Z_2).$$

19. A method as in claim 13 wherein the step of providing the oscillatory reference source further comprises the step of providing a crystal oscillator reference source.

20. A method as in claim 19 wherein the step of providing the crystal oscillator reference source further comprises the step of providing a 10MHz reference source.

21. A method as in claim 13 wherein the step of providing the oscillatory reference source further comprises the step of providing an atomic reference source.

22. A method as in claim 13 wherein the step of initializing the second counter further comprises the step of initializing the second counter at substantially the same time as initializing the first counter.

23. A method as in claim 13 wherein the step of partially correlating the transmitted signal further comprises the steps of:

providing one of the at least three PN component codes; and

correlating the one of the at least three PN component codes with the transmitted signal.

24. A method as in claim 23 wherein the step of determining the PN composite code slip for chip aligning further comprises the steps of:

providing a PN receiver clock source, the PN receiver clock source having a predetermined cycle rate;

using the PN receiver clock source to generate the at least three PN component codes, wherein the step of generating the at least three PN component codes further comprises the steps of:

initializing a receiver first counter, wherein the receiver first counter is adapted to count the PN receiver clock source cycles;

logically combining the at least three PN component codes to produce the PN composite code;

providing a receiver oscillatory reference source, the receiver oscillatory reference source having predetermined cycles;

initializing a receiver second counter, wherein the receiver second counter is adapted to count the cycles of the receiver oscillatory reference source;

determining a receiver delta phase in accordance with counts from the receiver first counter and the receiver second counter;

determining from the partially correlated signal the transmitter delta phase and the transmitter second counter count;

determining a latency associated with the receiver second counter; and

substantially aligning the receiver PN composite code with the transmitter PN composite code in accordance with a first function, the first function comprising the parameters: the transmitter delta phase, the transmitter second counter count, the receiver delta phase, the receiver second counter count, and the latency.

25. A method as in claim 24 wherein the step of logically combining the at least three PN component codes to produce the PN composite code further comprises the step of MAND combining the at least three PN component codes according to:

$$(X \oplus (Y \bullet (Z_1 \oplus Z_2)).$$

26. A method as in claim 24 wherein the step of logically combining the at least three PN component codes to produce the PN composite code further comprises the step of MAJ combining the at least three PN component codes according to:

$$(X \bullet Y) \oplus (X \bullet Z_1) \oplus (X \bullet Z_2) \oplus (Y \bullet Z_1) \oplus (Y \bullet Z_2) \oplus (Z_1 \bullet Z_2).$$

27. A method as in claim 24 wherein the step of providing the receiver oscillatory reference source further comprises the step of providing a crystal oscillator source.

28. A method as in claim 24 wherein the step of providing the receiver oscillatory reference source further comprises the step of providing a second atomic reference source.

29. A method as in claim 24 wherein the step of substantially aligning the receiver PN composite code with the transmitter PN composite code in accordance with the first function further comprises the steps of:

determining an uncertainty chip range associated with the latency associated with the receiver second counter;

moving the receiver generated PN code phases, other than the one receiver PN code used for partial correlation to a predetermined phase within the determined uncertainty chip range; and

searching for full correlation over the uncertainty range in units of a number of chips associated with the one receiver PN code used for partial correlation.

30. A system for generating (PN) spread signals, the system comprising:

a first clock generator;

at least three first pseudo-noise (PN) component code generators coupled to the first clock generator, wherein the first clock generator generates clock signals to drive the PN component code generators;

a logic combiner coupled to the outputs of the at least three first PN component code generators, the logic combiner adapted to generate a composite PN code;

a first N-bit counter coupled to the first clock generator, wherein the first N-bit counter counts the clock signals generated by the first clock generator;

a second clock generator, wherein the second clock generator is adapted to synchronize with the first clock generator; and

a second M-bit counter coupled to the second clock generator, wherein the second M-bit counter counts time since initialization of the second clock generator.

31. A system as in claim 30 wherein the first clock generator comprises a first direct digital synthesizer.

32. A system as in claim 30 wherein the logic combiner comprises a MAND logic combiner.

33. A system as in claim 30 wherein the logic combiner comprises a MAJ logic combiner.

34. A system as in claim 30 wherein the at least three first PN component code generators comprise four first PN component code generators.

35. An integrated circuit (IC), wherein the integrated circuit comprises:

a first clock signal generator for generating first clock signals;

at least three first pseudo-noise (PN) component code generators coupled to the first clock signal generator;

a logic combiner coupled to the output of the at least three first PN component code generators, the logic combiner adapted to generate a composite PN code;

a first N-bit counter coupled to the first clock signal generator, wherein the first N-bit

counter is adapted to count the first clock signals;

a second clock generator for generating second clock signals, wherein generating the second clock signals are synchronized with generating the first clock signals; and

a second M-bit counter coupled to the second clock generator, wherein the second M-bit counter is adapted to count time since initialization of synchronization of generating the second clock signals and generating the first clock signals.

36. An IC as in claim 35 wherein the first clock signal generator further comprises a first clock signal input pin.

37. An IC as in claim 36 wherein the first clock signal generator further comprises the first clock signal input pin coupled to a first direct digital synthesizer.

38. An IC as in claim 35 wherein the second clock generator further comprises a second clock signal input pin.

39. An IC as in claim 38 wherein the second clock generator further comprises the second clock signal input pin coupled to a second direct digital synthesizer.

40. An IC as in claim 38 wherein the second clock generator further comprises the second clock signal input pin coupled to an atomic clock.

41. An IC as in claim 38 wherein the second clock generator further comprises the second clock signal input pin coupled to a crystal oscillator.

42. An IC as in claim 35 wherein the first clock generator comprises an onboard first direct digital synthesizer.

43. An IC as in claim 35 wherein the second clock generator comprises an onboard second direct digital synthesizer.

44. An IC as in claim 35 wherein the second clock generator comprises an onboard first crystal oscillator.

45. An IC as in claim 35 wherein the IC comprises an Application Specific IC (ASIC).

46. An IC as in claim 35 wherein the IC comprises a field programmable gate array (FPGA).

47. A program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform method steps for generating and acquiring pseudo-noise (PN) composite spread signals, the method comprising the steps of:

at a transmitter:

providing a PN clock source, the PN clock source having a predetermined cycle rate;

using the PN clock source to generate at least three PN component codes, wherein the step of generating the at least three PN component codes further comprises the steps of:

initializing a first counter, wherein the first counter is adapted to count the PN clock source cycles;

logically combining the at least three PN component codes to produce a PN composite code;

providing an oscillatory reference source, the oscillatory reference source having predetermined cycles;

initializing a second counter, wherein the second counter is adapted to count the cycles of the oscillatory reference source;

determining a transmitter delta phase in accordance with counts from the first counter and the second counter;

PN composite coding the transmitter delta phase and the second counter count;

transmitting the PN composite coded transmitter delta phase and the PN composite second counter count at a predetermined rate;

at a receiver:

receiving the transmitted signal;

partially correlating the transmitted signal; and

determining a PN composite code slip for chip aligning a receiver PN composite code with the transmitter PN composite code.

48. A program storage device as in claim 38 wherein the program of instructions comprise at least one Very High Speed Integrated Circuit (VHSIC) Hardware Description (VHDL) Language file.